A Miniaturized X-band 4-Stage LNA Designed Using a Novel Layout Optimization Technique

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ABSTRACT

A novel layout optimization technique has been proposed and adapted to an X-band LNA. The layout pattern of the amplifier has been optimized in only two days by using simple equivalent circuits derived from electromagnetic simulation results. The amplifier has achieved a gain of 35 dB with a noise figure of 1.7 dB. These results have good agreement with simulated results, and the effective chip area is miniaturized to 4.8 mm^2.

INTRODUCTION

There have been several papers published describing monolithic low noise amplifiers (LNAs)[1-4]. Among them, monolithic microwave integrated circuits (MMICs) need to be improved in terms of noise performance and cost effectiveness to surpass hybrid MICs for communication systems, etc. Cost reduction for MMICs is particularly important for commercial applications. To achieve the low cost miniaturization of MMICs is an effective approach, and it can be achieved by using lumped elements[5] for matching networks.

However, in X-band and higher frequency ranges, it is difficult to make good use of lumped elements for matching networks because lumped elements have parasitic elements which degrade the circuit performance.

In miniaturizing MMICs consisting of distributed elements, the foremost consideration is to adjust performance simulated from the layout to target performance. The performance simulated from initial layout is different from the original design because of coupling effect between lines. The coupling effect between lines can be estimated accurately using an electromagnetic simulator (EM)[6-10]. However, the electromagnetic simulator does not give a clear guide to target performance.

In this study, we describe an optimization technique for an MMIC using distributed elements. The LNA with this technique has a gain of 35 dB with a noise figure of 1.7 dB for X-band using a self-aligned multi-layer gate FET (SAMFET)[11]. The effective chip area of the LNA is 4.8 mm^2.

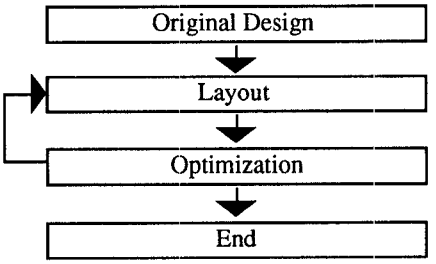

Fig. 1. Design process

OPTIMIZATION METHOD

In the optimization of the circuit layout, the procedure of EM analysis followed by modification of the layout is repeated until the simulated performance meets a target. However, there are some problems in this procedure: (i) There is no clear guide for modification of the layout. (ii) Much time is needed for the optimization.

In this amplifier design, therefore, we propose a novel approach in which the result of EM analysis is converted to an equivalent circuit. This approach gives a clear guide for the next layout. In the layout design, line widths and spaces of the pattern are kept constant for the purpose of representing each transmission line with a characteristic impedance and a line length without serious error. In addition, we use the same value of line width and space to shorten the simulation time in EM analysis. The basic circuit topology for EM analysis consists of three transmission lines which are connected to each other and are T shaped as a whole. As a result, characteristic impedance and line length of transmission line is decided easily by fitting.

Figure 1 shows the design process for the amplifier. In the original circuit design, transmission lines are only used as distributed elements. Next, pattern layout is performed so that the chip size is miniaturized. Finally, in an optimization step, the circuit layout is optimized to accomplish target performances using electromagnetic and circuit simulators.

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Figure 2 shows the optimization process for the circuit in detail. First, the initial pattern layout is conducted. At this stage, EM analysis is carried out for each pattern block by block. In this amplifier design, the circuit is divided into nine circuits which can be regarded as T-shaped.

After the EM analysis, the result is converted into a simple equivalent circuit for each part. The topology of the equivalent circuit is T-shaped, similar to the analyzed part of the original circuit. Fitting parameters are sets of width W_{em} and length P_{em}.

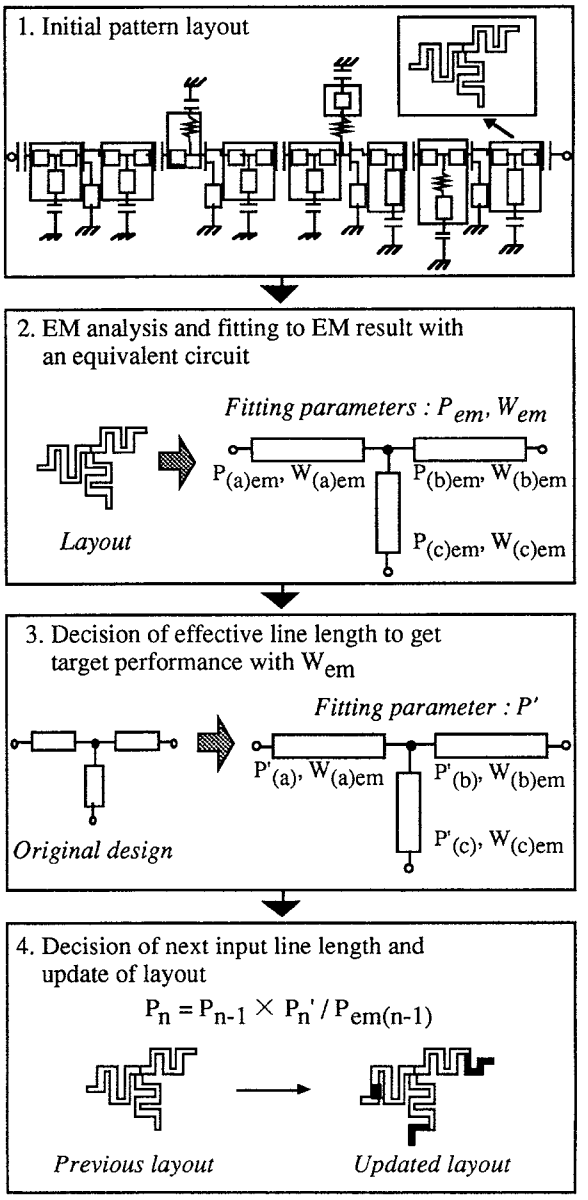
Next, the result of the original design is converted into a simple circuit with the same topology. The only parameter is line length P'. Line width is fixed to W_{em} which was decided at the previous step. At this step, the effective length of transmission lines for the target performance is estimated.

Next, input line length is decided using equation (1):

$$P_n = P_{(n-1)} \times P_n' / P_{em(n-1)} \qquad (1)$$

where n is the iteration number, P is the input line length, P_{em} is the line length of the result fitting the EM result, W_{em} is the line width of the result fitting the EM result, and P' is the line length of the result fitting the original design. At this time, line width is not updated because a large number of grid points is necessary for EM analysis and an unacceptably long time is spent for optimization.

In the case of this amplifier design, two or three iterations are needed to obtain a final layout. About two days are needed for the optimization. Figure 3 shows the results of the original design, calculated with the EM analysis from initial layout and final layout. The final results are not quite coincident with the original results. However, the optimization is stopped at the iteration satisfying with target performances.



n : Iteration number
P : Input line length
P_{em} : Line length of result fitting the EM result
W_{em} : Line width of result fitting the EM result
P' : Line length of result fitting the original design

Fig. 2. Optimization process

DEVICE DESCRIPTION AND CIRCUIT DESIGN

Figure 4 shows a cross sectional SEM photograph of the SAMFET. The gate metal consists of two layers. The under layer is WSi to obtain good reliability, and the upper layer is Au to obtain low gate resistance. The channel n-layer is formed by selective ion-implantation of Si into a 100 μm thick GaAs substrate. WSi gate films are deposited by sputtering. The gate films act as a mask for n+ and n'-implantation.

Each FET contained in this LNA has a gate size of 0.5 μm × 300 μm. The typical DC characteristics of these devices are an Idss (Vd = 3 V) of 40 mA with a pinch-off voltage of -0.5 V. Figure 5 shows measured maximum stable and available gain (MAG/MSG) versus frequency at Vd = 3 V, Id = 15 mA. The SAMFET has a maximum stable gain up to 25 GHz, an Fmin of 0.9 dB with an associated gain of 9.0 dB at 10 GHz.

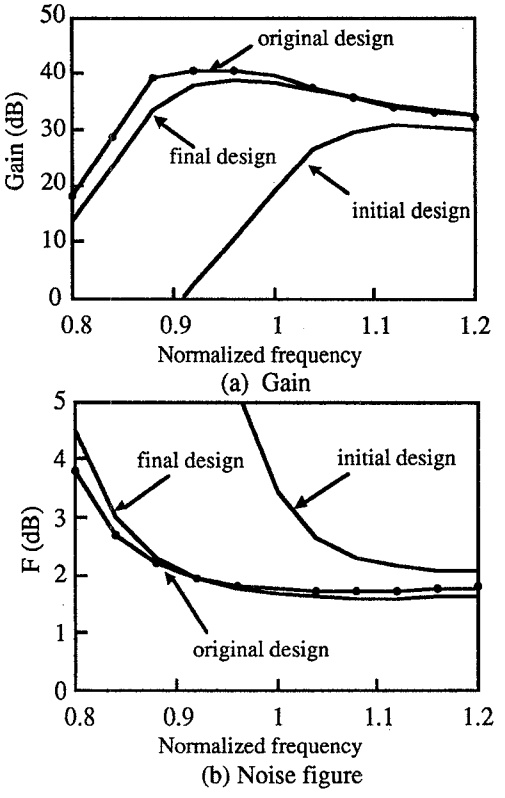


Fig. 3. The original design, the results calculated with the electromagnetic simulator from initial layout and final results.

Target performances for this amplifier was a noise figure of lower than 2.0 dB, a gain of 35 dB and VSWR of less than 2.0. A 0.5 μm × 300 μm SAMFET was used as an active device for each stage in the amplifier. Each SAMFET was biased at 3 V and 15 mA of Ids for good noise performance. Figure 6 shows a schematic diagram of the X-band 4-stage LNA MMIC. A 4-stage topology was selected to achieve the target noise figure and gain. In a first stage, the FET has external source inductance for optimum noise matching. In a second stage, FET has small external source inductance and the other FETs have feedback resistances as well as small source inductance for stable operation. The amplifier has two sets of trimming resistances for absorption of FET characteristics perturbation and simplicity of use.

RESULTS

Figure 7 shows a photograph of the X-band 4-stage MMIC LNA. The effective chip area except for trimming resistances and probing pads is 4.8 mm^2. Figure 8 shows the measured results of the amplifier compared with the final design. This amplifier achieved a gain of 35 dB with a noise figure of 1.7 dB. A good agreement between

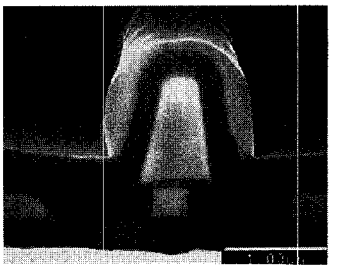


Fig. 4. A cross sectional SEM photograph of the SAMFET

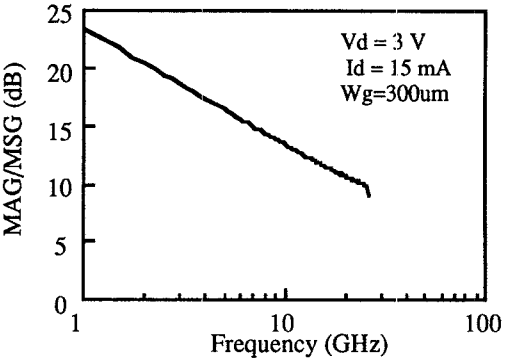


Fig. 5. Measured maximum stable and available gain (MAG/MSG) versus frequency

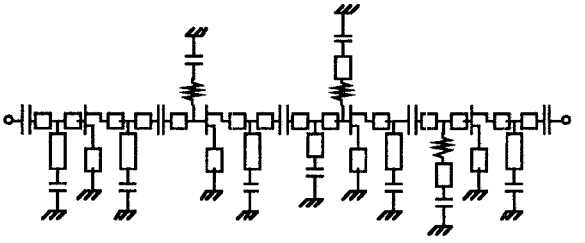


Fig. 6. A schematic diagram of an X-band 4-stage LNA MMIC

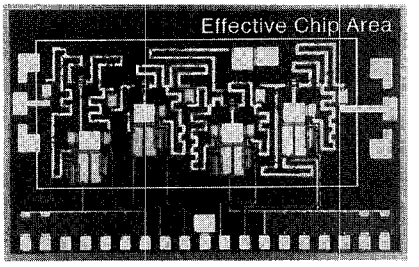


Fig. 7. A photograph of the X-band 4-stage MMIC LNA

measured and simulated data has been achieved.

CONCLUSION

An X-band 4-stage low noise amplifier has been developed. The amplifier has been designed using a novel optimization technique with an electromagnetic

simulator. The effective chip area except for trimming resistances and probing pads is 4.8 mm^2. The amplifier achieved a gain of 35 dB with a noise figure of 1.7 dB in the X-band. It has been demonstrated that this method is very effective for miniaturization of the chip area.

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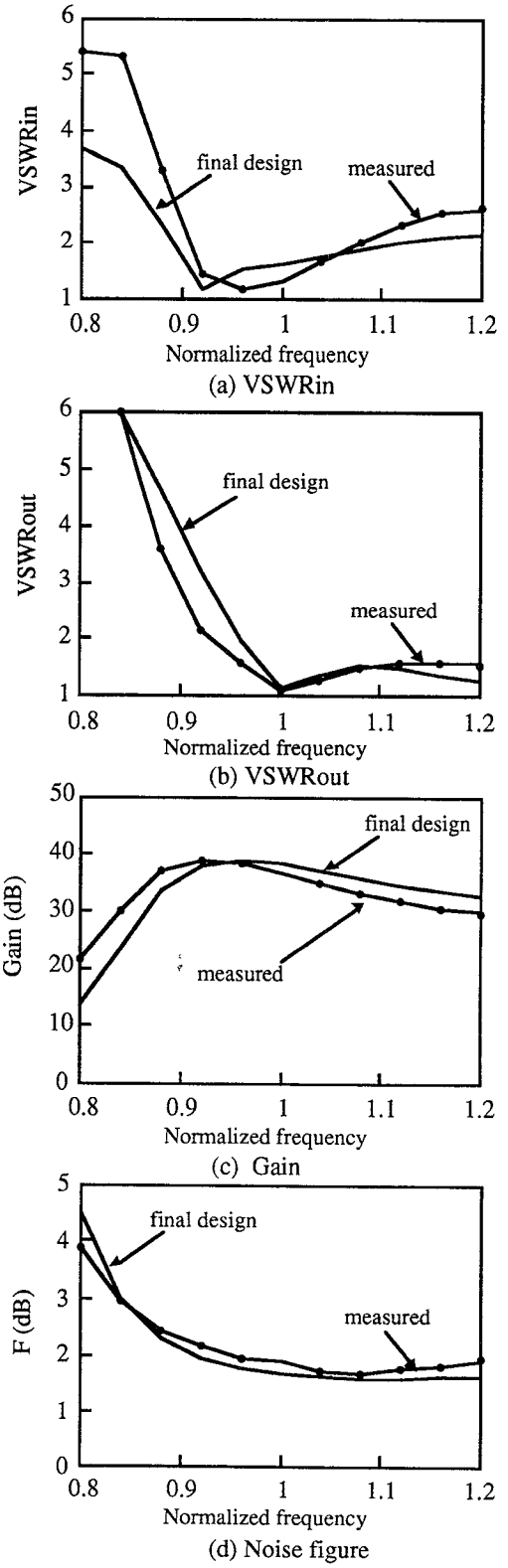

Fig. 8. Measured results of the amplifier compared with the final design